output a signal, and the semiconductor chip may further include an input/output buffer disposed within the semiconductor chip and configured to receive and/or output the signal, the input/output buffer being located corresponding to an input/output unit where the third pad is disposed, among the plurality of input/output units.

[0019] The semiconductor chip may further include at least one of: a first bump area connected to at least one of the first additional pad and the first pad through a first conductive line; a second bump area connected to at least one of the second additional pad and the second pad through a second conductive line; and a third bump area connected to a third pad through a third conductive line, the third pad disposed on a third row and configured to receive and/or output a signal.

[0020] The first conductive ring may be positioned to have a minimum distance from the first pad.

[0021] According to an aspect of still another embodiment, provided is a semiconductor chip including: a plurality of input/output units, wherein at least one input/output unit among the plurality of input/output units includes at least two from among: a first pad to which a ground voltage is applied; a second pad to which a power supply voltage is applied; and a third pad through which a signal is input and/or output.

[0022] In the at least one input/output unit, the at least two from among the first pad, the second pad, and the third pad may be disposed on different rows on a surface of the semiconductor chip.

[0023] The semiconductor chip may further include a plurality of pads disposed on the plurality of input/output units, wherein the plurality of pads include a plurality of first pads that are disposed on different rows on a surface of the semiconductor chip and/or a plurality of second pads that are disposed on different rows on the surface of the semiconductor chip.

[0024] The semiconductor chip may further include a conductive ring disposed within the semiconductor chip and electrically connected to the plurality of first pads and/or the plurality of second pads that are disposed on the different rows on the surface of the semiconductor.

BRIEF DESCRIPTION OF THE FIGURES

[0025] The above and/or other aspects will be more apparent by describing certain example embodiments with reference to the accompanying drawings.

[0026] FIG. **1** is a top plan view of a semiconductor chip in accordance with example embodiments.

[0027] FIG. **2** is a drawing illustrating an enlarged area of FIG. **1**.

[0028] FIG. **3** is a top plan view illustrating a part of a semiconductor chip in accordance with example embodiments.

[0029] FIG. **4**A is a cross-sectional view taken along the line A-A' of FIG. **3**.

[0030] FIG. **4**B is a cross-sectional view taken along the line B-B' of FIG. **3**.

[0031] FIG. **4**C is a cross-sectional view taken along the line C-C' of FIG. **3**.

[0032] FIG. **5**A is a cross-sectional view taken along the line D-D' of FIG. **3**.

[0033] FIG. **5**B is a cross-sectional view taken along the line E-E' of FIG. **3**.

[0034] FIG. **5**C is a cross-sectional view taken along the line F-F' of FIG. **3**.

[0035] FIG. **5**D is a cross-sectional view taken along the line G-G' of FIG. **3**.

[0036] FIG. **6** is a drawing illustrating a part of FIG. **3** in three dimensions.

[0037] FIG. **7** is a drawing illustrating a part of a semiconductor chip in accordance with other example embodiments.

[0038] FIG. **8** is a top plan view illustrating a part of a semiconductor chip in accordance with example embodiments.

[0039] FIG. **9**A is a cross-sectional view taken along the line A-A' of FIG. **8**.

[0040] FIG. **9**B is a cross-sectional view taken along the line B-B' of FIG. **8**.

[0041] FIG. **9**C is a cross-sectional view taken along the line C-C' of FIG. **8**.

[0042] FIG. **10**A is a cross-sectional view taken along the line D-D' of FIG. **8**.

[0043] FIG. **10**B is a cross-sectional view taken along the line E-E' of FIG. **8**.

[0044] FIG. **10**C is a cross-sectional view taken along the line F-F' of FIG. **8**.

[0045] FIG. **11** is a drawing illustrating a part of FIG. **8** in three dimensions.

[0046] FIG. **12** is a drawing illustrating a part of a semiconductor chip in accordance with other example embodiments.

[0047] FIG. **13** is a top plan view illustrating a part of a semiconductor chip in accordance with example embodiments.

[0048] FIG. **14**A is a cross-sectional view taken along the line A-A' of FIG. **13**.

[0049] FIG. **14**B is a cross-sectional view taken along the line B-B' of FIG. **13**.

[0050] FIG. **14**C is a cross-sectional view taken along the line C-C' of FIG. **13**.

[0051] FIG. **15**A is a cross-sectional view taken along the line D-D' of FIG. **13**.

[0052] FIG. **15**B is a cross-sectional view taken along the line E-E' of FIG. **13**.

[0053] FIG. **15**C is a cross-sectional view taken along the line F-F' of FIG. **13**.

[0054] FIG. **16** is a drawing illustrating a part of FIG. **13** in three dimensions.

DETAILED DESCRIPTION

[0055] Embodiments of inventive concepts will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This inventive concept may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope to those skilled in the art. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. Like numbers refer to like elements throughout.

[0056] It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected"